REMARKS

As a preliminary matter, the Examiner's withdrawal of claims 8, 16, 18 and 20 is respectfully traversed. These claims have already been indicated as generic in the Office Action dated October 2, 2003 so that Applicants' listing thereof is not necessary. Applicants' election dated October 30, 2003 indicated that at least claims 1-3 are readable on the particular elected *species* in addition to the claims already indicated by the Examiner as being *generic*. Accordingly, it is respectfully requested that claims 8, 16, 18 and 20 be examined as generic claims along with the claims listed as being drawn specifically to the elected species. Further, as claim 1 is believed patentable over the cited prior art for the reasons that follow, it is respectfully requested that all claims dependent thereon (directly or indirectly) be rejoined as being dependent on an allowable claim.

Claim 3 stands objected to for alleged minor informalities. The Examiner asserts that the recitation "when the pixel transistor is in its non-continuity state" is irrelevant to length. This is incorrect. The Examiner is directed to, for example, page 33, last line – page 34, line 8 of Applicants' specification corresponding to Figure 3, which describes one exemplary embodiment of a periphery 182 or 183 which depends on the state of the pixel transistor (compare claims 3 and 4). Accordingly, it is respectfully requested that the objection to claim 3 be withdrawn.

Claims 1-3 stand rejected under 35 U.S.C. § 112, first paragraph (enablement). This rejection is respectfully traversed for the following reasons. The Examiner appears to base this

rejection on the assertion that a periphery length of a gate electrode to pixel electrode capacitor (represented as "Lgd") "may mean any number of possibilities." It is respectfully submitted that the Examiner's allegation is directed to claim *scope* rather than claim enablement and is therefore irrelevant to making a determination with respect to enablement. The Examiner is directed to MPEP § 2164.08 under the heading "Enablement Commensurate in Scope With the Claims", which sets forth the applicable standard:

> As concerns the breadth of a claim relevant to enablement, the only relevant concern should be whether the scope of enablement provided to one skilled in the art by the disclosure is commensurate with the scope of protection sought by the claims. (citing *In re Moore*, 169 USPQ 236, 239 (CCPA 1971).

In the instant case, the Examiner has not asserted that one skilled in the art could not make and use any one or more of the possibilities listed by the Examiner. The Examiner instead alleges that the claim language covers many possibilities and assumes that this claim breadth renders the claims non-enabled. However, claim breadth by itself does not render claims non-enabled. Rather, claim scope which covers non-enabled embodiments can render that claim non-enabled, notwithstanding the claim may also cover enabled embodiments. Accordingly, it is respectfully submitted that the rejection under § 112, first paragraph is *per se* improper because the Examiner has not asserted that any of the listed possibilities is non-enabled by Applicants' specification.

Nonetheless, it is further submitted that the Examiner's allegation that the "periphery length of the gate electrode to pixel electrode capacitor, designated by Applicant as 'Lgd' is not adequately defined in the Specification" is incorrect. The Examiner is again directed to, for example, page 33, last line – page 34, line 8 of Applicants' specification corresponding to Figure 3, which describes two exemplary embodiments of Lgd corresponding to two peripheries 182 and 183, depending on the state of the pixel transistor. It is respectfully submitted that one of

ordinary skill in the art having Applicants' specification and the disclosed exemplary embodiments, coupled with knowledge known in the art (e.g., defining capacitor peripheries), would readily know how to make and use the full scope of the present invention as recited in the pending claims.

Based on all the foregoing, it is respectfully submitted that claims 1-3 are fully enabled. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 112, first paragraph be withdrawn.

Claims 1-3 stand rejected under 35 U.S.C. § 103 as being unpatentable over Watanabe et al. '793 ("Watanabe") in view of Park et al. '347 ("Park"). This rejection is respectfully traversed for the following reasons.

A. Proposed combination does not disclose claimed invention

Claim 1 recites in pertinent part, "a storage capacitor provided ... for holding a voltage applied between its corresponding pixel electrode and the opposed electrode" (emphasis added). In contrast, the alleged storage capacitor 419 of Watanabe holds a voltage between its corresponding pixel electrode and the capacitor line 423.

The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in claim 1 because the proposed combination fails the "all the claim limitations" standard required under § 103.

B. Proposed combination and modification are improper

The Examiner admits that Watanabe does not disclose the claimed "index B" and apparently relies on Park as evidence that "index B" being equal to or greater than 7 would have been an obvious modification based on MPEP § 2144.05 (II), which sets forth that discovering an optimum or workable range by routine experimentation involves only routine skill in the art. However, it is respectfully submitted that the Examiner's reliance on MPEP § 2144.05 (II) is improper because the Examiner has not established that the parameters defining the index B are result-effective variables. The Examiner merely concludes that such is the case. The Examiner is directed to MPEP § 2144.05(II)(B) under the heading "Only Result-Effective Variables Can Be Optimized", which sets forth the applicable standard for determining result-effective variables:

> A particular parameter must first ***be recognized*** as a result-effective variable, i.e., a variable which achieves a recognized result, before the determination of the optimum or workable ranges of said variable might be characterized as routine experimentation. (citing *In re Antonie*, 195 USPQ 6 (CCPA 1977)).

In the instant case, Park is completely silent as to the peripheries of the storage capacitor and gate-to-pixel capacitor, let alone the ratio thereof defining index B as achieving a recognized result. Indeed, as set forth by the Examiner, Park is directed merely to increasing storage capacitance generally, and does so "by increasing the area of overlap between the gate line and subsidiary electrode" (*see* col. 4, lines 30-33). At best, therefore, Park has recognized "the area of overlap between the gate line and subsidiary electrode" as a result-effective variable that can be optimized by routine experimentation.

Only Applicants have discovered that the claimed index B can provide a recognized result, and provided the motivation and method to determine the claimed value thereof. Applicants' specification goes into great detail in this regard (*see, e.g.,* page 23, line 8+ of

Applicants' specification). Because Park is completely silent as to the ratio of the peripheries defining the index B, pursuant to the cited MPEP section above, optimum or workable ranges of the index B can NOT be characterized as routine experimentation. Indeed, Park does not provide any motivation or rationale for experimenting to reach the claimed index B.

Moreover, it is respectfully submitted that Park does not provide the necessary teachings ***to enable*** one of ordinary skill in the art to reach the claimed index B. For example, when the area of the storage capacitor electrode is two-dimensionally increased, the periphery of the storage capacitor is increased. However, in Park, the area of the storage capacitor electrode is not two-dimensionally increased but rather is three-dimensionally increased by using the lateral surfaces in the gate line as the surface of the electrode. Accordingly, the periphery of the storage capacitor is not increased (*see* Figs. 4-7). Therefore, Park does not enable, let alone provide any suggestion or motivation for, one of ordinary skill in the art to modify Watanabe so as to increase the periphery of the storage capacitor.

Further, as disclosed at col. 2, lines 31-35 of Park, it is difficult to increase the area of the storage capacitor electrode (subsidiary electrode) of the LCD of the related art due to the structural limitations. Therefore, as described on page 29, line 24 - page 30, line 20 of Applicants' specification, Lst/Lgd (=index B) is usually from 3 to 4 with about 6 as a maximum in the conventional LCD. Therefore, from this point of view as well, it is not possible based on the teachings of Park for one of ordinary skill in the art to modify Watanabe so as to set Lst/Lgd (=index B) to be equal to or greater than 7.

On the other hand, only Applicants' specification provides the motivation and means by which to reach the claimed invention. For example, turning to page 30, lines 7-14 of Applicants' specification, the capacitance of the storage capacitor can not be increased without limit but is

determined relative to the liquid crystal capacitance, unlike in the description of Park. Accordingly, in an exemplary embodiment of the present invention, the pattern (contour) of the periphery of the storage capacitor can be transformed to allow the periphery thereof to be increased. By doing so, the long periphery of the storage capacitor can be actually obtained. In contrast, Park is silent as to such a process and indeed does not suggest nor provide motivation for transforming the pattern of the periphery of the storage capacitor. Again, for this additional reason, it is not possible based on the teachings of Park for one of ordinary skill in the art to modify Watanabe so as to allow the periphery of the storage capacitor to be actually increased.

For all the foregoing reasons, it is respectfully submitted that the cited prior art does not suggest nor enable the present invention as recited in claim 1.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on all the foregoing, it is submitted that claims 1-3 are patentable over Watanabe in view of Park. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 103 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicant submits that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: May 27, 2004